AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 8, line 1, with the following rewritten paragraph.

-- Accordingly, according to the correction principle, a delay time td1 ~~dt1~~ at the rise of the logical level immediately after the horizontal blanking period T is made short compared to the case where the dummy data DD is not at all inserted, thereby solving the problem that delay time varies according to the length of the immediately preceding logical level. More specifically, if the dummy data DD is inserted in this manner, the logical level of the input data is forcedly switched and the period during which the logical level of the input data is held at a logical L level can be made short compared to the case where the dummy data DD is not at all inserted, so that a variation in delay time can be reduced in a data string of the input data D1. Accordingly, it is possible to effectively avoid latching of erroneous data and the like. --

Please replace the paragraph beginning at page 13, line 29, with the following rewritten paragraph.

-- Fig. 11 is a connection diagram showing the down converter 24. The down converters 24 and 25 are identically configured except that data to be processed by them is different. In what follows, reference is made to the configuration of only the ~~latch circuit~~ down converter 24, but a description as to the ~~latch circuit~~ down converter 25 is omitted. --